UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,792	07/10/2003	Shuzo Fujioka	009683-470	3507

7590 07/06/2006

BURNS, DOANE, SWECKER & MATHIS, L.LP.
P.O. Box 1404
Alexandria, VA 22314-1404

EXAMINER	
ALMEIDA, DEVIN A	

ART UNIT	PAPER NUMBER
2191	

DATE MAILED: 07/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,792	FUJIOKA, SHUZO	
	Examiner	Art Unit	
	Devin Almeida	2191	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the papers filed 7/10/2003 with the benefit of the filing date of Japan Patent Application No. 2002-380316 filed 12/27/2002. Claims 1-15 were received for consideration. No preliminary amendments for the claims were filed. Currently claims 1-15 are under consideration.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-9, 11, 12, and 15 are rejected under 35 U.S.C. 102(e) and 35 U.S.C. 102(a) as being anticipated by Asami et al (U.S. Pub. # 2003/0014643). Asami teaches claim 1, an information security microcomputer having an information security function comprising (see paragraph 0002). An encrypting unit encrypting and decrypting information (see paragraph 0023 and paragraph 0029), an authenticating unit (see paragraph 0019 i.e. authorization device) authenticating an external device (see figure 2 element 4 electronic device paragraph and 0019), and a processor (see figure 1 element 2-2 CPU) performing entire control of said information security microcomputer

(See figure 1 element 2 LSI and see paragraph 0017), and stopping at least a part of a function of said information security microcomputer when said authenticating unit cannot perform the authentication (see paragraph 0022-0025).

With respect to claim 2, wherein said processor issues a random number to said external device, decrypts information received from said external device, and attempts to authenticate said external device by determining whether the decrypted value matches with said random number or not (see figure 2 and paragraph 0022-0025).

With respect to claim 3, wherein said processor stops an entire operation of said information security microcomputer when said authenticating unit cannot perform the authentication (see paragraph 0022-0025 i.e. paragraph 0024 lines 5-9).

With respect to claim 4, wherein said processor stops an operation of said encrypting unit when said authenticating unit cannot perform the authentication (see paragraph 0022-0025 i.e. paragraph 0024 lines 5-9).

With respect to claim 5, wherein said processor operates not to output a correct result of an operation of said encrypting unit when said authenticating unit cannot perform the authentication (see paragraph 0022-0025 i.e. paragraph 0024 lines 5-9).

With respect to claim 6, wherein said processor operates in either a debug mode (see figure 3 i.e. s124 Debug Function Enable and paragraph 0034 lines 6-9) or a general mode (see figure 3 i.e. s126 Debug Function Disable and paragraph 0032 lines 9-11), and said information security microcomputer further includes a mode-lock circuit locking the mode at debug mode (see paragraph 0034 i.e. once authenticates it become

possible to use the debugging functions otherwise it get locks and it is not possible to use the debugging functions).

With respect to claim 7, an information security microcomputer having an information security function (see paragraph 0002), and a main body controlling said information security microcomputer to assist program development (see figure 1 element 1 ICE, element 3 Authorization Device, and element 4 Electronic Device), wherein said main body includes a control unit performing authentication with respect to said information security microcomputer (see figure 4 element 3 Authorization Device), and issuing a command to control said information security microcomputer (see paragraph 0022 line 3-8 i.e. command data). Said information security microcomputer includes, an authenticating unit performing authentication with respect to said main body (see element 3 Authorization Device and paragraph 0018), and a processor (see figure 1 element 2-2 CPU) performing entire control of said information security microcomputer, and stopping at least a part of a function of said information security microcomputer (see paragraph 0022-0025).

With respect to claim 8, an information security microcomputer (See figure 1 element 2 LSI and see paragraph 0017) having an information security function (see paragraph 0002), a main body (see figure 1 element 1 ICE, element 3 authorization device, and element 4 electronic device) controlling said information security microcomputer to assist program development and a computer issuing a command to said information security microcomputer via said main body (see paragraph 0019). Wherein authentication is performed between at least two of said information security

microcomputer, said main body and said computer (See figure 2 authorization between authorization device (main body) and LSI (information security microcomputer)).

With respect to claim 9, wherein said information security microcomputer (See figure 1 element 2 LSI and see paragraph 0017) includes, an encrypting unit encrypting and decrypting information (see paragraph 0023 and paragraph 0029), an authenticating unit (see paragraph 0019 i.e. authorization device) authenticating said main body or said computer (see paragraph 0019), and a processor (see figure 1 element 2-2 CPU) performing entire control of said information security microcomputer, and stopping at least a part of a function of said information security microcomputer (See figure 1 element 2 LSI and see paragraph 0017) when said authenticating unit cannot perform the authentication (see paragraph 0022-0025).

With respect to claim 11, wherein said main body performs authentication with respect to said computer (see paragraph 0019), and control is performed to stop an operation of at least a part of a function of said main body when the authentication cannot be performed (see paragraph 0022-0025).

With respect to claim 12, wherein said main body performs authentication with respect to said computer and authentication with respect to said information security microcomputer (see paragraph 0019), and control is performed to stop an operation of at least a part of a function of said information security microcomputer or said main body when the authentication cannot be performed (see paragraph 0022-0025).

With respect to claim 15, further comprising, a network connecting said computer to said main body (see figure 2 element 6 interface board), wherein said computer

sends a program after encrypting said program when said program is to be downloaded into said main body, and said main body executes said encrypted program received from said computer after decrypting said encrypted program (see paragraph 0041).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asami et al (U.S. Pub. # 2003/0014643) in view of Daggar (U.S. Patent # 5,748,737). The Asami reference teaches everything in claim 8 as stated above but with respect to claim 10 does not teach the authentication performed between at least two of said information security microcomputer, said main body and said computer is repeated at predetermined intervals. The Foster reference teaches the authentication performed between at least two of said information security microcomputer, said main body and said computer is repeated at predetermined intervals (see column 19 line 59 – column 20 line 2). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have to perform authentication at predetermined intervals since the Foster reference teaches that it would provide an extra security measure (see column 20 lines 1-2). Since it checks to see that the two devices are still authenticated.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asami et al (U.S. Pub. # 2003/0014643) in view of Foster et al (U.S. Patent # 5,652,890). The Asami reference teaches everything in claim 8 as stated above but with respect to claim 13 does not teach, the said computer receives authentication information from a user, and sends the authentication information to said information security microcomputer, said information security microcomputer determines whether the authentication information received from said computer matches with authentication information held in advance by said information security microcomputer or not, and said computer performs control not to operate at least a part of a function of said main body when said information security microcomputer determines mismatch of said authentication information. The Foster reference teaches the said computer receives authentication information from a user, and sends the authentication information to said information security microcomputer (see column 29 lines 58-61), said information security microcomputer determines whether the authentication information received from said computer matches with authentication information held in advance by said information security microcomputer or not (see column 29 lines 61-66), and said computer performs control not to operate at least a part of a function of said main body when said information security microcomputer determines mismatch of said authentication information (see column 29 line 61 – column 30 line 4). There for it would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have included a password in addition to the

authentication process to help make sure help make sure the authentication between two devices to secure.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asami et al (U.S. Pub. # 2003/0014643) in view of Foster et al (U.S. Patent # 5,652,890) and in further view of Affeldt et al (U.S. Patent # 5,620,519). The Asami in view of Foster et al teaches everything in claim 13 as stated above but with respect to claim 14 does not teach the computer requesting a user to reenter the authentication information if input by the user is not performed for a predetermined time or more. The Affeldt reference teaches the computer requests a user to reenter the authentication information if input by the user is not performed for a predetermined time or more (see column 13 line 27-35). There for it would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have to have included the user to reenter the authentication information if input by the user is not performed for a predetermined time. This make it so you can leave the computer while it is running and not worry about someone accessing any of the functions.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Devin Almeida whose telephone number is 571-270-1018. The examiner can normally be reached on Monday-Thursday from 7:30 A.M. to 5:00 P.M. The examiner can also be reached on the second Fridays of the pay cycle from 7:30 A.M. to 4:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Robertson, can be reached on 571-272-4186. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DA

Devin Almeida
Patent Examiner
June 20, 2006

DAVID L. ROBERTSON
PRIMARY EXAMINER